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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/067,424	02/07/2002	Jeng Ping Lu	7447.0021-01	8498

22852 7590 09/02/2003

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
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EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/067,424	LU ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 7 – 9, 11 – 13, and 15 – 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) in view of Miki et al. (USPAT 5499207) Possin et al. (USPAT 5777355, Possin).

With regard to claim 7, the AAPA discloses in figure 2 a method for making a high fill factor image array (40). The AAPA discloses in figure 2 providing a plurality of source-drain metal contacts (44). The AAPA discloses in figure 2 depositing a first passivation layer (first three quarters of the thickness of 56 deposited on 42). The AAPA discloses on page 2, lines 19 – 20 that a preferred material for the first passivation layer is silicon oxynitride. The AAPA also discloses on page 3, lines 11 – 18 that an interface with the silicon oxynitride and an overlying layer causes conducting channels to occur between two lateral pixel electrodes. The AAPA further discloses on page 3, lines 19 – 21 a material different than silicon oxy-nitride as a first passivation layer is advantageous to prevent the conducting channels from forming between two pixel electrodes. However, the AAPA does not discuss using a second passivation layer overlying the first passivation layer to prevent the conducting channels from forming between two pixel electrodes. Miki teaches in figures 5a – 5f and column 4, lines 55 – 66 depositing a

second passivation layer (103) that suppresses lateral leakage current. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the second passivation layer of Miki in the method of the AAPA in order to provide electric isolation between electrodes (104) which overly the passivation layer as stated by Miki in figures 1 and 5a – 5f, column 3, lines 10 – 20 and column 4, lines 55 – 66. Further, any processing occurring after the deposition of the first passivation layer in the AAPA will now occur after the deposition of the first and second passivation layers. It should be noted that the limitation of "that suppresses lateral leakage current" is an intended use recitation that bears to patentable weight in a method claim. The AAPA discloses in figure 2 (taken together with the teaching of Miki) opening a plurality of via holes through the first and second passivation layers. The AAPA discloses in figure 2 depositing a layer of conductive material. The AAPA discloses in figure 2 depositing a first doped a-Si layer (48). The AAPA discloses in figure 2 patterning to form the collection electrodes (46). The AAPA discloses in figure 2 (taken together with the teaching of Miki) depositing a continuous layer of i a-Si (50) disposed on the second passivation layer. The AAPA discloses in figure 2 depositing a continuous second layer of doped a-Si (52). The AAPA discloses in figure 2 depositing an upper conductive layer (54). It is not clear if the AAPA and Miki teach patterning the upper conductive layer. Possin teaches in figures 1 and 2; and in the abstract depositing and patterning an upper conductive layer (28). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the patterning step of Possin in the method of the AAPA and Miki in order to differentiate the device into a plurality of devices, thus creating an array, which results in cost savings over having to make a plurality of devices separately.

With regard to claim 11, the AAPA discloses in figure 2 a high fill factor image array (40) forming process. The AAPA discloses in figure 2 providing a plurality of source-drain metal contacts (44). The AAPA discloses in figure 2 depositing a first passivation layer (first three quarters of the thickness of 56 deposited on 42). The AAPA discloses on page 2, lines 19 – 20 that a preferred material for the first passivation layer is silicon oxynitride. The AAPA also discloses on page 3, lines 11 – 18 that an interface with the silicon oxynitride and an overlying layer causes conducting channels to occur between two lateral pixel electrodes. The AAPA further discloses on page 3, lines 19 – 21 a material different than silicon oxy-nitride as a first passivation layer is advantageous to prevent the conducting channels from forming between two pixel electrodes. However, the AAPA does not discuss using a second passivation layer overlying the first passivation layer to prevent the conducting channels from forming between two pixel electrodes. Miki teaches in figures 5a – 5f and column 4, lines 55 – 66 depositing a second passivation layer (103) that suppresses lateral leakage current. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the second passivation layer of Miki in the method of the AAPA in order to provide electric isolation between electrodes (104) which overly the passivation layer as stated by Miki in figures 1 and 5a – 5f, column 3, lines 10 – 20 and column 4, lines 55 – 66. Further, any processing occurring after the deposition of the first passivation layer in the AAPA will now occur after the deposition of the first and second passivation layers. It should be noted that the limitation of "that suppresses lateral leakage current" is an intended use recitation that bears to patentable weight in a method claim. The AAPA discloses in figure 2 (taken together with the teaching of Miki) opening a plurality of via holes through the first and second passivation layers. The AAPA

discloses in figure 2 depositing a layer of conductive material. The AAPA discloses in figure 2 depositing a first doped a-Si layer (48). The AAPA discloses in figure 2 patterning to form the collection electrodes (46). The AAPA discloses in figure 2 (taken together with the teaching of Miki) depositing a continuous layer of i a-Si (50) disposed on the second passivation layer. The AAPA discloses in figure 2 depositing a continuous second layer of doped a-Si (52). The AAPA discloses in figure 2 depositing an upper conductive layer (54). It is not clear if the AAPA and Miki teach patterning the upper conductive layer. Possin teaches in figures 1 and 2; and in the abstract depositing and patterning an upper conductive layer (28). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the patterning step of Possin in the method of the AAPA and Miki in order to differentiate the device into a plurality of devices, thus creating an array, which results in cost savings over having to make a plurality of devices separately.

With regard to claim 16, the AAPA discloses in figure 2 a method for making a high fill factor image array (40). The AAPA discloses in figure 2 providing a plurality of source-drain metal contacts (44). The AAPA discloses in figure 2 depositing a first passivation layer (first three quarters of the thickness of 56 deposited on 42) over the source-drain metal contact. The AAPA discloses on page 2, lines 19 – 20 that a preferred material for the first passivation layer is silicon oxy-nitride. The AAPA also discloses on page 3, lines 11 – 18 that an interface with the silicon oxy-nitride and an overlying layer causes conducting channels to occur between two lateral pixel electrodes. The AAPA further discloses on page 3, lines 19 – 21 a material different than silicon oxy-nitride as a first passivation layer is advantageous to prevent the conducting channels from forming between two pixel electrodes. However, the AAPA does not discuss

using a second passivation layer overlying the first passivation layer to prevent the conducting channels from forming between two pixel electrodes. Miki teaches in figures 5a – 5f and column 4, lines 55 – 66 depositing a second passivation layer (103) over a first passivation layer (102). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the second passivation layer of Miki in the method of the AAPA in order to provide electric isolation between electrodes (104) which overly the passivation layer as stated by Miki in figures 1 and 5a – 5f, column 3, lines 10 – 20 and column 4, lines 55 – 66. Further, any processing occurring after the deposition of the first passivation layer in the AAPA will now occur after the deposition of the first and second passivation layers. The AAPA discloses in figure 2 (taken together with the teaching of Miki) opening a via hole through the first and second passivation layers to expose the source-drain metal contact. The AAPA discloses in figure 2 depositing a layer of conductive material (46) on the source-drain metal contact, such that the layer of conductive material makes electrical contact with the source-drain metal contact. The AAPA discloses in figure 2 depositing a first doped a-Si layer (48) on the layer of conductive material. The AAPA discloses in figure 2 patterning the a-Si layer and the layer of conductive material to form a collection electrode (46). The AAPA discloses in figure 2 (taken together with the teaching of Miki) depositing sensor material comprising a continuous layer of i a-Si (50)over the collection electrode and at least a portion of the second passivation layer. The AAPA discloses in figure 2 depositing a continuous layer of doped a-Si (52) over the continuous layer of i a-Si. The AAPA discloses in figure 2 depositing a conductive layer (54) over the continuous layer of doped a-Si. The AAPA discloses in figure 2 that the conductive layer is an upper electrode. It is not clear if the AAPA teaches patterning the upper conductive layer to

form the upper electrode. Possin teaches in figures 1 and 2; and in the abstract depositing and patterning a conductive layer (28) to form an upper electrode. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the patterning step of Possin in the method of the AAPA in order to differentiate the device into a plurality of devices, thus creating an array, which results in cost savings over having to make a plurality of devices separately.

With regard to claims 8, 12, and 17, the AAPA discloses in figure 2 and page 2, line 19 wherein the first passivation layer comprises silicon oxynitride.

With regard to claims 9, 13, and 18, Miki discloses in column 5, lines 14 – 16 wherein the second passivation layer is an oxide.

With regard to claim 15, the APPA discloses in figure 2 wherein the thickness of the second passivation layer is less than the thickness of the first passivation layer.

3. Claims 10, 14, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the AAPA, Miki and Possin as applied to claims 7, 11, and 16 above, and further in view of one of ordinary skill in the art.

With regard to claims 10, 14, and 19, Miki discloses in column 5, lines 14 – 16 wherein the second passivation layer has a thickness of about 100 Å. The AAPA, Miki and Possin do not teach wherein the second passivation layer has a thickness of about 1000 Å. According to MPEP 2144.05 II.A optimization through routine experimentation is obvious. In this case it would have been obvious to one of ordinary skill in the art at the time of the present invention to use a

second passivation layer thickness of about 1000 Å in order to use a thickness which is consistent with the dimensions and electrical characteristics of the device being made.

Response to Arguments

4. Applicant's arguments with respect to claims 7 – 19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
August 20, 2003